



[0018] In another embodiment of the present invention, the metal hard-mask film and the bit line metal film are formed using the same metal material.

[0019] In another embodiment of the present invention, the metal hard-mask film is formed using tungsten (W) with a thickness in the range of 500 Å to 1000 Å to endure significantly as an etching barrier in the subsequent process of etching the interlayer insulation film.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0020] The above and other objects, advantages and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with accompanying drawings, in which:

[0021] Fig. 1 is a cross-sectional view illustrating a problem due to a decrease in a pattern size between bit lines of the conventional flash device;

[0022] Fig. 2 is a lay-out diagram illustrating a problem due to a conventional method of forming a bit line of a flash device;

*CL* [0023] Figs. 3A <sup>thru</sup> and 3C are cross-sectional views taken along II-II' line in Fig. 2;

[0024] Fig. 4 is a lay-out diagram showing a bit line of a flash device according to the present invention; and,

[0025] Figs. 5A to 5D are cross-sectional views taken along V-V' line in Fig. 4 for the purpose of illustrating a method for forming a bit line of a flash device according to the present invention.

### **DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

[0026] Now, embodiments of the present invention will be described in detail with reference to accompanying drawings. However, present invention is not limited to the embodiments disclosed in the following description, but can be implemented into various changes and modifications. Thus, these embodiments according to the present invention are intended to inform those skilled in the art of a scope of the present invention. The same component in the drawings is referred to the same numeral.

[0027] Shown in Fig. 4 is a lay-out diagram showing a bit line of a flash device according to the present invention. Referring to Fig. 4, a bit line B/L pattern is formed using a patterning process on a semiconductor substrate, on which word line W/L, DSL, SSL, and bit line contact plug 112 are formed. The bit line B/L of the present invention are allowed to constantly hold an interval between target bit lines by controlling conditions of a hard-mask